IN THE SPECIFICATION:

IN THE CLAIMS:

1. (currently amended) A method of forming an integrated circuit ~~an~~ on a substrate having a set of vertical field effect transistors having a channel in a carbon nanotube, comprising the steps of:

forming a first conductive layer on a substrate;

forming a first insulating layer on said first conductive layer; and

forming a gate layer on said first insulating layer having a gate ~~insulator~~ thickness within a thickness tolerance of less than 5%, three sigma;

forming a set of apertures, having substantially vertical interior walls, through said gate layer and said first insulating layer, the bottom of said aperture exposing said first conductive layer;

forming an insulating liner on said walls of said aperture;

after said step of forming an insulating liner, forming a set of semiconductive carbon nanotubes in said apertures ~~by~~ ;

introducing a chemical constituent into the nanotube material during formation of only one of the top and bottom of the nanotube to produce an electrical effect during operation, the bottom of said carbon nanotube being in electrical contact with said first conductive layer; and

forming an electrical contact on a top of said carbon nanotube.

2. (original) A method according to claim 1, further comprising the steps of:

forming a set of at least two apertures through said gate layer and connecting the bottoms of the set of carbon nanotubes in said set of apertures in parallel to said first conductive layer, thereby forming a set of FETs having a common electrode in said first conductive layer and a common gate electrode.

3. (original) A method according to claim 1, further comprising the steps of:

forming a layer of catalyst on said bottom of said aperture, such that said catalyst initiates the growth of a semiconductor carbon nanotube.

4. (original) A method according to claim 1, further comprising the steps of:

forming said insulating liner by thermally oxidizing said gate layer.

5. (original) A method according to claim 1, further comprising the steps of:

forming said insulating liner by chemical vapor deposition.

6. (Canceled)

7. (currently amended) A method according to claim 1 ~~6~~, in which said chemical constituent is introduced to suppress short channel effects during transistor operation.

8. (original) A method according to claim 2, further comprising the steps of:

forming a layer of catalyst on said bottom of said aperture, such that said catalyst initiates the growth of a semiconductor carbon nanotube.

9. (original) A method according to claim 2, further comprising the steps of:

forming said insulating liner by thermally oxidizing said gate layer.

10. (original) A method according to claim 2, further comprising the steps of:

forming said insulating liner by chemical vapor deposition.

11. - 14. (canceled)

15. (original) A method according to claim 3, further comprising the steps of:

introducing a chemical constituent into the nanotube material during formation of one of the top and bottom of the nanotube to produce an electrical effect during operation.

16. (original) A method according to claim 15, in which said chemical constituent is introduced to suppress short channel effects during transistor operation.

17. (Withdrawn) A vertical field effect transistor having a channel in a carbon nanotube, comprising:

a first conductive layer disposed on a substrate;

a first insulating layer disposed on said first conductive layer; and

a gate layer disposed on said first insulating layer;

an aperture, having substantially vertical interior walls, extending through said gate layer and said first insulating layer, the bottom of said aperture exposing said first conductive layer;

an insulating liner on said walls of said aperture;

a semiconductive carbon nanotube in said aperture, the bottom of said carbon nanotube being in electrical contact with said first conductive layer; and

an electrical contact formed on a top of said carbon nanotube.

18. (Withdrawn) A transistor according to claim 17, further comprising: a set of at least two apertures through said gate layer, the bottoms of the set of carbon nanotubes in said set of apertures being connected in parallel to said first conductive layer, thereby forming a set of FETs having a common electrode in said first conductive layer and a common gate electrode.

19. (Withdrawn) A transistor according to claim 17, further comprising: a layer of catalyst on said bottom of said aperture, such that said catalyst initiates the growth of a semiconductor carbon nanotube.

20. (Withdrawn) A transistor according to claim 17, further comprising: a chemical constituent introduced into the nanotube material

during formation of one of the top and bottom of the nanotube to produce an electrical effect during operation.